AMENDMENTS TO THE CLAIMS

1. (Currently amended) A method of processing a memory read request from a central processing unit (CPU) of a microprocessor, the method comprising:

~~retrieving into the microprocessor~~ retrieving, into the microprocessor, a cache tag associated with the memory read request from a cache memory bank that is external to the microprocessor, wherein the cache memory bank stores cache tags and cache data in separate memory locations;

within the microprocessor, comparing the cache tag to a memory address associated with the memory read request to assess whether data requested by the CPU resides within the cache memory bank; and

subsequent to retrieving the cache tag from the cache memory bank into the microprocessor, retrieving the cache data associated with the memory read request from the cache memory bank into the microprocessor, whereby the retrieval of the cache data into the microprocessor does not overlap in time with the retrieval of the cache tag into the microprocessor;

wherein the cache tag and the cache data are retrieved in sequence from the cache memory bank over a common set of bus lines that connect the microprocessor to the cache memory bank, such that at least one bus line of the common set of bus lines is used to retrieve both the cache tag and the cache data.

2. (Previously presented) The method of Claim 1, wherein the step of accessing the cache memory bank to retrieve said data overlaps in time with said step of comparing the cache tag to the memory address.

3. (Canceled)

4. (Original) The method of Claim 1, further comprising comparing the cache tag to the memory address within a system controller device that interfaces the microprocessor to a main memory.

5. (Original) The method of Claim 1, wherein the method comprises mapping the memory address into a cache tag address and a cache data address that are sequentially provided to the cache memory bank to retrieve the cache tag and the cache data therefrom.

6. (Previously presented) The method of Claim 5, wherein mapping the memory address comprises using an address mapping function that subdivides a memory space of the cache memory bank into separate cache tag locations and cache data locations.

7. (Previously presented) The method of Claim 1, wherein the method comprises using an address transformation circuit of the microprocessor to convert the memory address into separate cache memory addresses for reading the cache tag and cache data from the cache memory bank.

8. (Currently amended) A microprocessor system, comprising:

a bank of general purpose random access memory that stores both cache tags and cache data in separate memory locations, said general purpose random access memory lacking cache tag comparison circuitry; and

a microprocessor connected to the bank of general purpose random access memory, and configured to use the bank of general purpose random access memory as an external cache memory;

wherein the microprocessor is configured to retrieve a cache tag from the bank of general purpose random access memory before retrieving corresponding cache data from the bank of general purpose random access memory, and is configured to retrieve the cache tag and the corresponding cache data from the bank of general purpose random access memory over a common set of bus lines such that at least one bus line of the common set of bus lines is used to retrieve both the cache tag and the corresponding cache data..

9. (Previously presented) The microprocessor system of Claim 8, wherein the microprocessor implements an address mapping function to map a memory address into a cache tag address and a cache data address for retrieving the cache tag and cache data from the bank of general purpose random access memory, said cache tag address and cache data address being distinct from each other.

10. (Previously presented) The microprocessor system of Claim 8, wherein the microprocessor retrieves cache tags and cache data from the bank of general purpose random access memory over a shared address/data bus such that cache tag accesses are not performed in parallel with cache data accesses.

11. (Original) The microprocessor system of Claim 8, wherein the microprocessor includes a comparison circuit that compares the cache tag to an associated memory address to determine whether data requested by a CPU of the microprocessor resides within the bank of general purpose random access memory.

12. (Previously presented) The microprocessor system of Claim 8, wherein the microprocessor includes an address transformation circuit that transforms a memory read address into a cache tag address and a separate cache data address, and is configured to use the cache tag address, followed in time by the cache data address, to sequentially retrieve the cache tag and the cache data from the bank of general purpose random access memory.

13. (Currently amended) A microprocessor, comprising:

a central processing unit that supplies a memory address for performing a memory read operation;

an address transformation circuit that translates the memory address supplied by the central processing unit into a first address for retrieving a cache tag from an external cache memory, and into a second address for retrieving cache data from the external cache memory, the second address being different from the first address, wherein the microprocessor is configured to use the first address to retrieve the cache tag from the external cache memory, and to then use the second address to retrieve the cache data from the external cache memory; and

a comparison circuit that compares the memory address supplied by the central processing unit and the cache tag retrieved from the external cache memory to assess whether said cache data is valid.

14. (Previously presented) The microprocessor of Claim 13, wherein the microprocessor is configured to compare the cache tag to the memory address with said comparison circuit while the cache data is being retrieved from the external cache memory.

15. (Previously presented) The microprocessor of Claim 13, wherein the microprocessor is configured to use the second address to perform a sequence of memory read operations to retrieve said cache data from the external cache memory.

16. (Previously presented) The microprocessor of Claim 15, wherein the microprocessor is configured to abort said sequence of memory read operations when a comparison performed by the comparison circuit reveals that the cache data is not valid.

17. (Previously presented) The microprocessor of Claim 13, wherein the address transformation circuit subdivides an addressable memory space of the external cache memory into a plurality of cache tag locations and a plurality of cache data locations.

18. (Previously presented) The microprocessor of Claim 17, where the number of said cache data locations is approximately three times the number of said cache tag locations.

19. (Previously presented) The microprocessor of Claim 13, wherein the microprocessor is configured to use a single bank of general purpose random access memory as said external cache memory.

20. (Previously presented) The microprocessor of Claim 13, in combination with the external cache memory, wherein the external cache memory consists of a single memory array that stores both cache tags and cache data in separate locations.

21. (Previously presented) The microprocessor of Claim 13, wherein the microprocessor uses the external cache memory as a level 2 cache.

22. (Currently amended) The microprocessor of Claim 13, wherein the microprocessor **[[in]]** is configured to retrieve the cache tag and the cache data from the external cache memory over a common set of bus lines.

23. (Previously presented) The microprocessor of Claim 13, wherein the address transformation circuit uses a first address transformation function to generate the first address and uses a second address transformation function to generate the second address.

24. (Previously presented) The microprocessor of Claim 13, wherein the address transformation circuit is configured to map a main memory space into a set of cache tag addresses and a set of cache data addresses, wherein the set of cache tag addresses and the set of cache data addresses are mutually exclusive such that cache tags and cache data may be stored in a common memory array.

25. (Previously presented) The microprocessor of Claim 24, wherein the set of cache data addresses is larger than the set of cache tag addresses.

26. (Previously presented) The microprocessor system of Claim 8, wherein the microprocessor is configured to use a first transformation function to map a main memory space into a set of cache tag addresses, and to use a second transformation function to map the main memory space into a mutually exclusive set of cache data addresses, and wherein the microprocessor is further configured to use the cache tag addresses and cache data addresses to access the bank of general purpose random access memory.

27. (Previously presented) The microprocessor system of Claim 26, wherein the set of cache data addresses is larger than the set of cache tag addresses.

28-35: (Canceled)